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GB 1349104
GB 1226473
GB 1186127
GB 1179805
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(58) Field of search
B1S

(54) A process for fabricating a semiconductor material and an apparatus therefor

(57) A silicon single crystal ingot (5) not separated from its seed (5a) is suspended in an upright position within the bell jar (1) of an upright type annealing furnace by clamping the seed (5a) in a chuck (7) on the bell jar (1). The ingot (5) is annealed by radiant heat which is emitted from infrared lamps (6) disposed around the outer circumference of the bell jar (1). The ingot (5) is held such that no part of the portion of its body which will provide a wafer is in contact with the apparatus. The annealing temperature is 1,200°C or higher. After this annealing treatment, the ingot is cooled to 1,100°C at a rate of 10 to 15°C/min. and further to 300°C at a rate of 25 to 100°C/min. and is held at 300°C for a predetermined time period. By the cooling treatment from 1,100°C to 300°C, it is made possible to suppress generation of microdefects and oxygen donors.

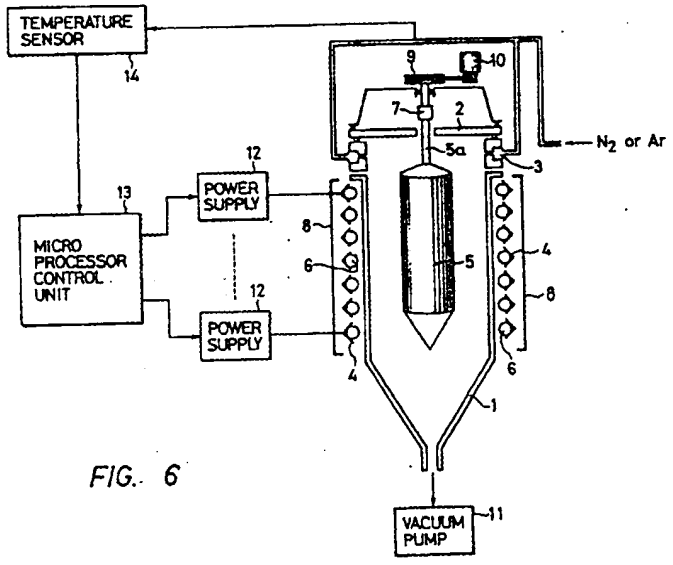

FIG. 6

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2137524

FIG. 1

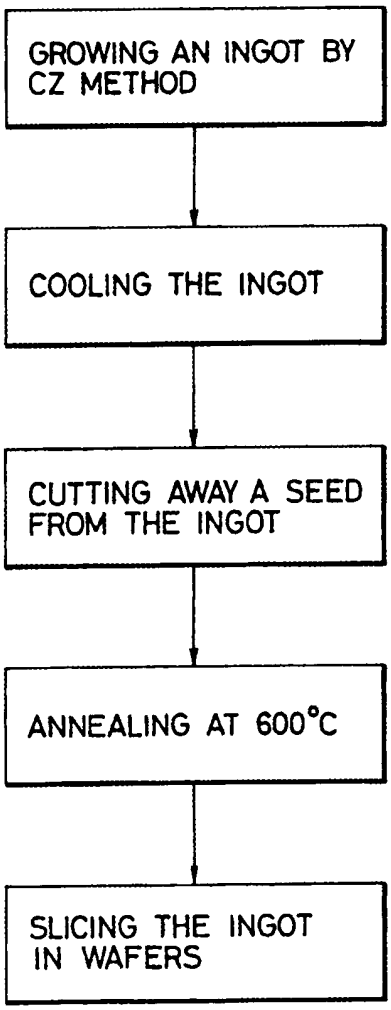


FIG. 5

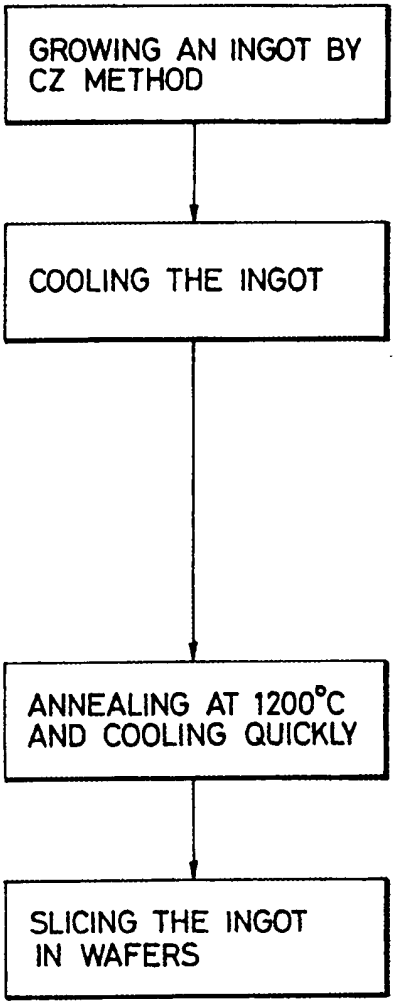
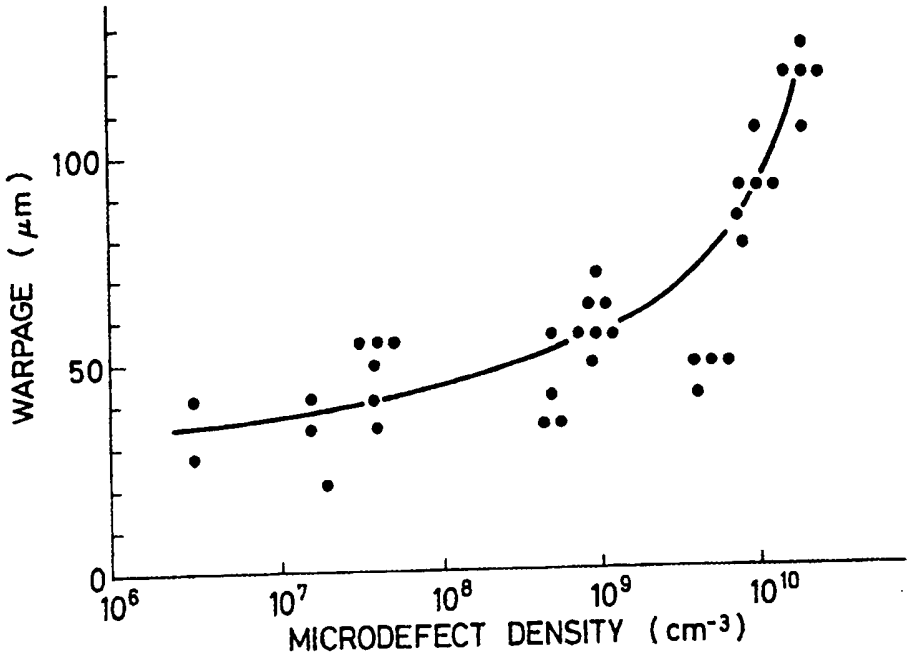


FIG. 2


WARPAGE (μm)
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50
0
10^6
10^7
10^8
10^9
10^10
MICRODEFECT DENSITY (cm^-3)

FIG. 7

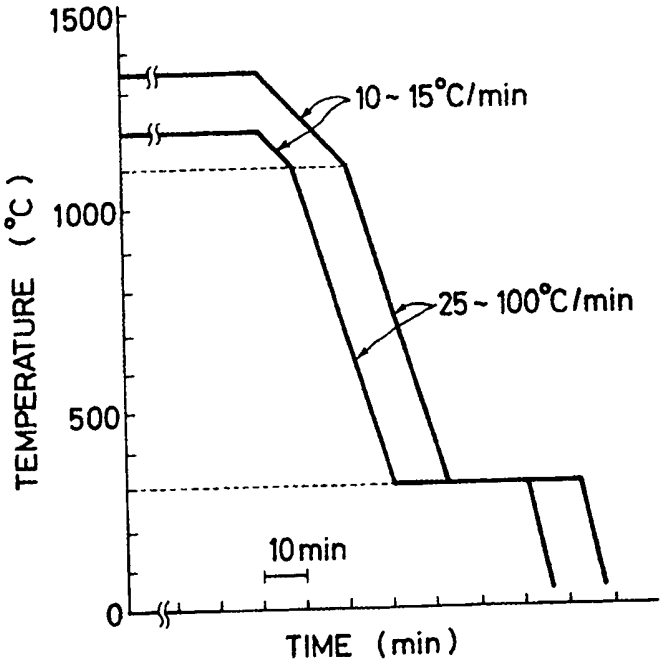
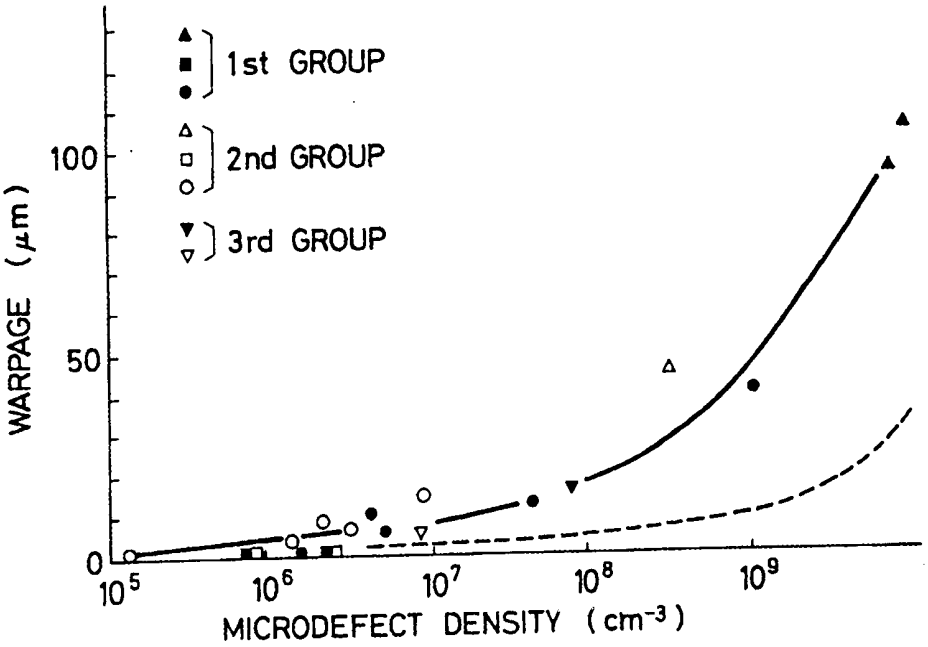

1500
1000
500
0
TEMPERATURE (°C)
10~15°C/min
25~100°C/min
10min
TIME (min)

FIG. 3


1st GROUP
2nd GROUP
3rd GROUP
WARPAGE (μm)
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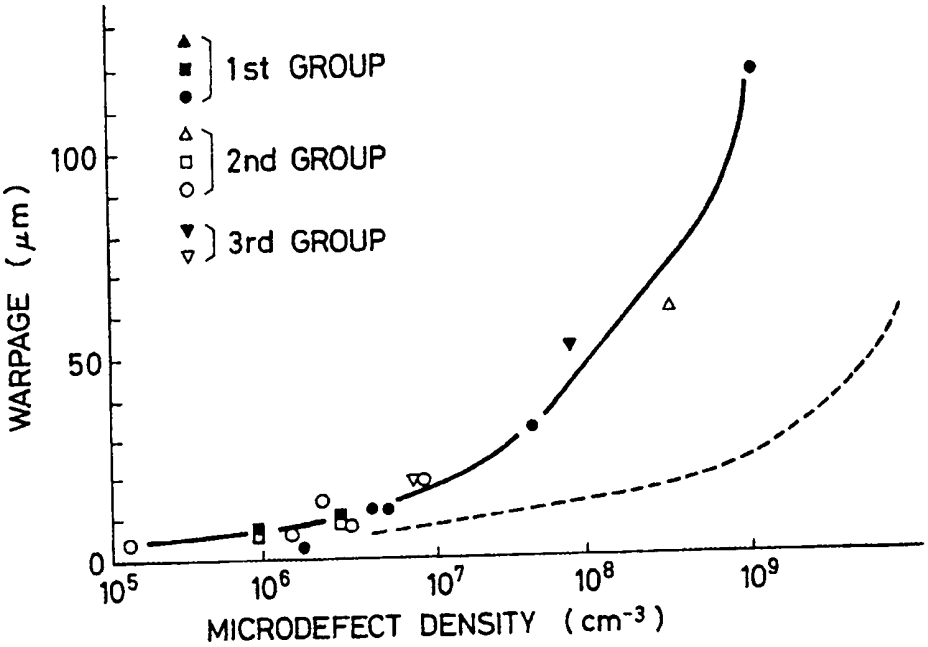
50
0
10^5
10^6
10^7
10^8
10^9
MICRODEFECT DENSITY (cm^{-3})

FIG. 4


1st GROUP
2nd GROUP
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MICRODEFECT DENSITY (cm^{-3})

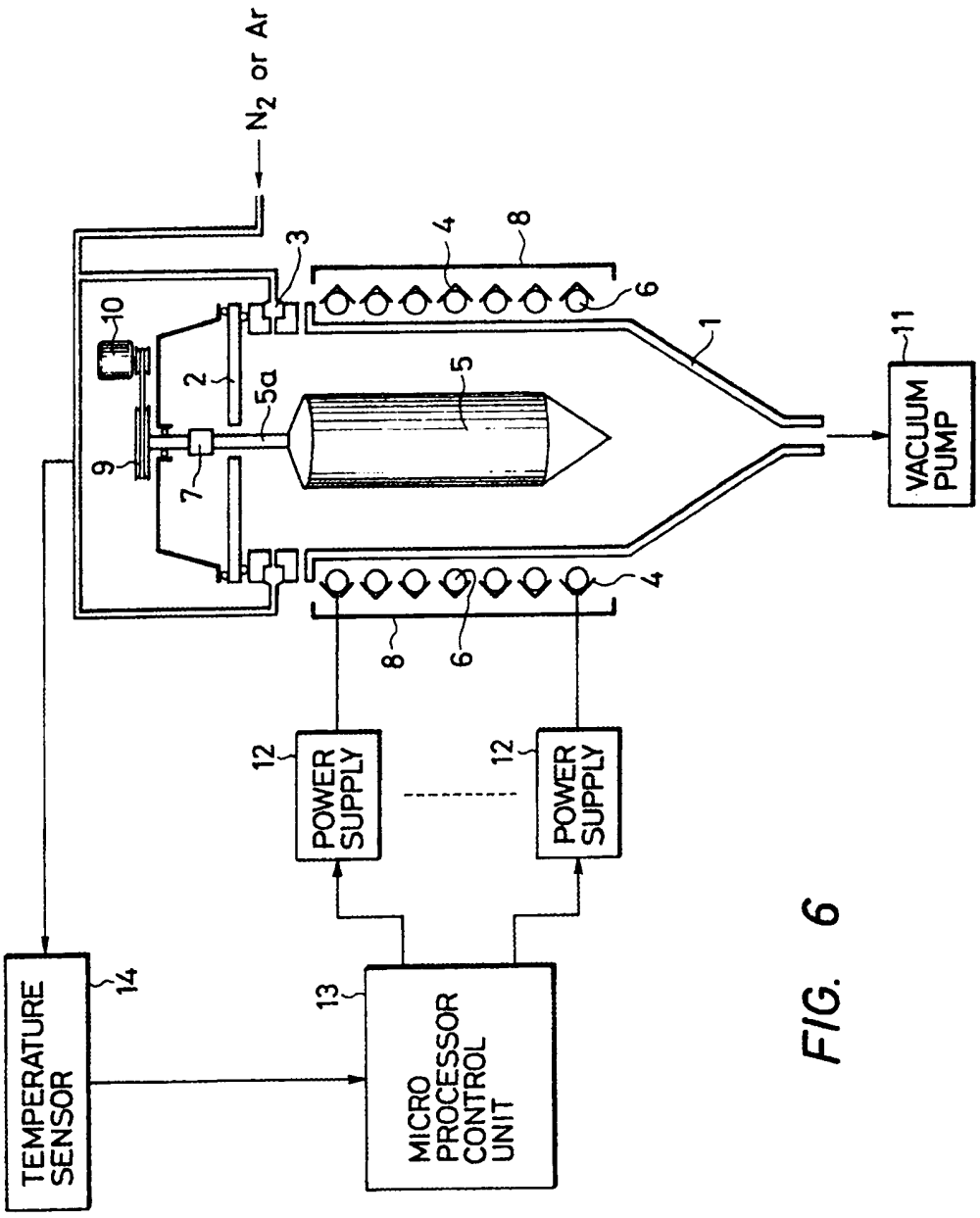
N_2 or Ar
3
4
8
6
1
10
2
5a
5
11
VACUUM PUMP
9
7
4
8
6
12
POWER SUPPLY
12
POWER SUPPLY
14
TEMPERATURE SENSOR
13
MICRO PROCESSOR CONTROL UNIT

FIG. 6

SPECIFICATION

A process for fabricating a semiconductor material and an apparatus therefor

The present invention relates to a process for fabricating a semiconductor material, and to an apparatus for carrying out such a process.

The Czochralski method (i.e. the CZ method) and the float-zone method are known in the art as methods of growing a silicon single crystal, which provides the principle material for semiconductor devices.

Most wafers to be used in silicon devices, such as LSI devices, at present are grown by the following CZ method. Polycrystalline silicon is melted in a quartz crucible. A seed immersed in the molten silicon is withdrawn upwardly whilst being rotated relative to the crucible, to grow the crystal.

A single crystal ingot grown by the CZ method has many microdefects or their cores. The growth states and numbers of the microdefects or their cores are different in different portions of the ingot. As a result, there is a variation in quality in the wafers, which are prepared by slicing an ingot grown by the CZ method. These problems are caused by the CZ method itself and are inevitable.

The cores of the microdefects are based on impurities such as carbon or heavy metals (e.g., gold, iron or copper) or on centres of stress concentration may be made by differences in the temperature distribution in the ingot. They are generated inside the ingot during growth. Ingots made by the CZ method contain oxygen atoms at a density of about 10^{18} atoms/cm^3. This value exceeds the solid solution limit, e.g., 3×10^{17} atoms/cm^3 at 1000°C. Oxygen in excess over the solid solution limit concentrates in the microdefect cores thereby generating microdefects. The term "microdefects" in this specification mean crystal defects of several micrometres or smaller and include e.g., oxide precipitates, stacking faults and small dislocation loops. The part of the ingot which has most recently been grown has a significantly high temperature. As a result, oxygen concentrates at the microdefect cores, generating precipitates of 10 to 50 Å during the growth of the crystal.

The number of microdefects and their cores are larger at the seed side (or top side) of the ingot than at the opposite side (or tail side). This is due to the oxygen and impurity concentrations in the ingot, which derive from the segregation factor. Furthermore, the number of microdefects and their cores differ due to the thermal history of the ingot in a drawing-up furnace, as a result of fluctuations in the temperature at the interface between the liquid and solid phases during the drawing-up operation.

Microdefects cause dislocations. The microdefects and the dislocations deteriorate the electric characteristics of the devices and cause reduction in the production yield. In recent years, high integration and performance of semicondutor devices has been advancing, and the problem of controlling the crystal defects caused by microdefects is one of the most interesting ones in the process control. In a solid image pickup element, for example, the presence of crystal defects forms white points in the image and is the principle cause of a reduction in the yield.

Thus a major problem in the fabrication of semiconductor devices is that there are many microdefect cores in an ingot grown by the CZ method and that there is significant dispersion in the distribution of the microdefect cores.

The present invention seeks to provide a process for fabricating a semiconductor material in which the formation of microdefects and their cores may be reduced. This is achieved by heating the semiconductor material by radient heat and then cooling it. The use of radient heat reduces the generation of microdefect cores and enables more uniform heating, reducing the risk of cracking of the semiconductor material. It also makes possible the heat treatment of the material without contacting the material, further reducing the risk of damage to the material. it is desirable that the material is heated to at least 0.85 to 0.95 T where T is the melting point of the semiconductor material.

During cooling of the semiconductor material, it is desirable to use a two step cooling operation, in which the material is first cooled slowly from its original high temperature to a temperature of e.g., 1100°C then rapidly cooled at the rate of 25 to 100°C/min to a temperature not greater than 380°C.

The present invention also provides an apparatus for fabricating a semiconductor material having a radient heat source preferably formed by a plurality of infrared lamps which surround a container for the semiconductor material.

Embodiments of the invention will now be described in detail, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a flow chart showing the conventional steps for annealing an ingot;

Figure 2 is a graph plotting the relationship between the warpage of a wafer and the microdefect density;

Figure 3 is a graph plotting the relationship between the warpage of a wafer by a forced heat treatment and the microdefect density;

Figure 4 is a graph plotting the relationship between the microdefect density and the warpage of a wafer by another forced heat treatment;

Figure 5 is a flow chart showing the steps for annealing an ingot by a process according to the present invention;

Figure 6 is a schematic section showing one embodiment of a semiconductor fabricating apparatus according to the present invention; and

Figure 7 is a time chart illustrating the temperature programs for the annealing step and the quick cooling step of the present invention.

First, experiments carried out by the inventors of the present invention concerning the effect of microdefects will be described.

The first experiment examined how microdefect cores are changed by the conventional ingot annealing treatment.

This ingot annealing treatment is performed to reduce the variation in resistivity in the direction of growth and in the section of the ingot which

corresponds to a wafer, by eliminating oxygen donors in the ingot. The oxygen donors appear at 450°C. Therefore the conventional ingot annealing treatment is carried out within a temperature range of 600 to 650 °C.

The conventional ingot annealing treatment follows the steps shown in Figure 1. An ingot cut away from a seed is laid on a boat. The ingot is then annealed in a non-oxidizing atmosphere within a horizontal type heat treating furnace.

Comparisons were made at annealing temperatures of 600°C, 650°C and 700°C. It was also found that the defect density of the wafer is higher at higher annealing temperatures. It was found that the conventional ingot annealing treatment promotes the generation of microdefect cores.

It was also found that the conventional ingot annealing treatment is not desirable when the ingot has a diameter of 125mm or larger. This is due to the fact that the ingot is so bulky that it has high internal stresses and requires a long annealing time, thereby promoting the generation of cores. Moreover, the annealed ingot has to be cooled quickly in air at a rate of 50 to 80°C/min. So as to reduce the rate of change of the resistivity. However, this quick cooling treatment cannot be used because cracks are generated in the ingot.

The relationship between the warpage of the wafer and the microdefect density was examined in the second experiment.

Figure 2 plots the relationship between the warpage of wafers with a diameter of 100 mm and the density of microdefects. The wafers were actually formed with complementary MOSFETs by the 5μm process.

It can be seen from Figure 2 that the warpage of the wafers increases with increasing microdefect density. The warpage of the wafers was measured after the source and drain regions of the MOSFETs had been formed. The measurement of the warpage were conducted by the laser interference method.

The microdefect density was measured by using conventional method, in which the microdefect density in the wafer bulk is examined. The wafers are oxidized at 1,000°C for 16 hours, mirror-polished to a depth of 40 μm, and etched with Wright etching liquid for 5 minutes. The number of defects at predetermined positions are countered and converted into the bulk density (numbers/cm^3).

If the warpage exceeds 70 μm, the accuracy of transfer of a pattern from a photolithographic mask to the wafer during photolithography is degraded, even if the 5 μm process is used so that the yield of the elements is accordingly reduced.

The microdefect density has to be equal to or less than 5×10^8 cm^{-3}. Even if the microdefect density in the bulk is increased, to obtain an intrinsic gettering effect, densities higher than 5×10^9 cm^{-3} would reduce so much that the benefits of the gettering effect would be lost.

It is necessary to reduce warpage with the increasing density of integration on semiconductor integrated circuits.

Figures 3 and 4 plot the relationships between the warpage of the wafers and the microdefect density. No electronic devices are formed on the wafers used. The methods of measuring the warpages of the wafers in the diametrical direction and the microdefect densities are the same as those of Figure 2.

In the experiments under consideration, the initial warpages of the wafers are subtracted from those after the respective heat treatments. The initial warpages are generated when the ingot is sliced and are at maximum about 25 μm. As a result, the warpages indicate the net values which come from elastic deformation during heat treatment.

In the examples shown in Figures 3 and 4, the wafers belonging to the first group are heat-treated at 800°C in a dry O_2 atmosphere for 2 hours and then at 1,000°C in an oxidizing atmosphere for 16 hours. The heat treatment at 800°C increases the likelihood of the generation of microdefect cores. The latter heat treatment at 1,000°C tends to generate microdefects and anticipates the generation of microdefects similar to those generated in the actual process of forming electronic devices in the wafer. The wafers of the second group are subjected only to heat treatment at 1,000°C. The wafers of the third group are not heat-treated, but are presented for comparison.

In the example shown in Figure 3, the wafers belonging to the first and second groups are subjected to a first forced heat treatment to allow evaluation of the warpages. The wafers are arranged vertically in a boat at spacings of 5 mm. The boat containing the wafers is inserted into the quartz tube of a horizontal type heat treating furnace. The quartz tube has an internal diameter of 150 mm and has an inside temperature of 1,000°C. The wafers in the quartz tube remain for 20 minutes and are then extracted. The boat is brought into and out of the quartz tube at a speed of 20 cm/min. by an autoloader.

In the example shown in Figure 4, the wafers of the first and second groups are subjected to a first forced heat treament to evaluate warpage and then to a second forced heat treatment. This second forced heat treatment is identical to the first one except that the boat speed is 35cm/min. The stresses in the wafers are higher for the second forced heat treatment.

The broken curves appearing in Figures 3 and 4 indicate the results which were obtained from the comparison wafers sampled from the ingot under different growing conditions.

From Figures 3 and 4, the following facts may be determined. The warpages are generally proportional to the density of microdefects. From comparisons of the wafers of the first and second groups and the comparisons of Figures 3 and 4, it is found that the density of microdefects increases and the warpages are more liable to occur with increasing heat treatment. In other words, the wafers are liable to warp due to the higher thermal stress in the wafers. These tendencies are found in any wafer, and may be high or low.

The microdefect density changes with the temperature of the heat treatment of the semiconductor material. This change is caused by the change in the

oxygen concentration in the crystal. Microdefects cause dislocations. These dislocations increase with increasing microdefect density. As a result, the critical stress is reduced and hence the slips or steps formed in the wafer surface by the concentration of multiple dislocations, are also reduced. Wafers having a higher density of microdefects are liable to have slips or warpages because of heat treatment during the LSI process. This degrades the transfer accuracy of patterns from photolithographic masks to the wafers during photolithography.

This implies that the core formation and growth of the microdefects and the likelihood of slips occurring are different if the oxygen concentration in the crystal changes.

The warpages from thermal stress are highly dependent upon the quality of the single crystal, particularly upon the precipitation of oxygen (i.e., the microdefect density).

In order to reduce the thermal stress causing warpages, the Ramping process may be carried out during the heat treatment of the wafer. According to the experiments of the inventor of the present invention, if the Ramping process is carried out at a temperature of 800 to 900°C, cores of oxygen precipitates are liable to be generated, and the microdefects are likely to grow so that the crystal's strength is deteriorated.

As a result, a uniform crystal is required such that oxygen is not precipitated even by heat treatment and that few microdefect cores are generated.

Figure 5 is a flow chart showing the procedures of the semiconductor material fabricating process which may be used in a process according to the present invention. the ingot of a single silicon crystal, which has been prepared by the CZ method, is transferred to an annealing furnace, as shown in Figure 6, without having its seed separated. The handling of the ingot is carried out in a state where all the seed portions are clamped in suspended positions by a chuck. The ingot is annealed in the annealing furnace in accordance with the temperature programmes illustrated in Figure 7.

The annealing heat treatment furnace shown in Figure 6 has an upright structure having a transparent quartz bell jar 1. this bell jar 1 has its top sealed by means of a cover 2. An upright type furnace is used to keep the body of the ingot from coming into contact with the apparatus.

The quartz bell jar 1 is filled via a gas inlet 3 with a non-oxidizing atmosphere gas, i.e., an inert gas such as nitrogen or argon. Before introduction of the gas, the bell jar 1 is evacuated to a high vacuum by means of a vacuum pump 11. The bell jar 1 is shaped to be similar to that of an open ingot 5 so that the gas is distributed uniformly therein.

The quartz bell jar 1 is loaded with the ingot 5, made of a silicon single crystal. The ingot 5 is clamped above the quartz bell jar 1 by means of a chuck 7 so that it can rotate at a speed of 0 to 30 r.p.m. The seed 5a of the ingot 5 is not cut away from the ingot 5, but instead remains attached to it. This is one of the features of the present embodiment. The chuck 7 clamps the seed 5a.

The body of the ingot 5, i.e., the portion to be formed into the wafers, is prevented from contacting the apparatus. Contaminants exisiting on the inner wall of the bell jar 1 are kept away from the ingot 5. The fact that there is no contact with the ingot 5, and hence no mechanical stresses generated by such contact, prevents the formation of minute cracks on the ingot surface. Also there is no change in the temperature of the ingot, which could occur by the transfer of heat to the apparatus if there was any contact. The outside of the ingot, therefore, plays no part in generating microdefects, cracks and contaminants in the ingot body. The formation of microdefects can then be controlled by controlling only the annealing temperature.

The chuck 7 is connected to a pulley 9 which in turn is coupled to a motor 10 by means of an endless belt. The ingot is rotated to ensure that temperatures or changes in temperature at the respective portions of the ingot are uniform.

In the apparatus of the present embodiment, a radiant heat source is used as the annealing heat source. This radiant heat source is provided by infrared lamps 6. These infrared lamps 6 are arranged outside of the quartz bell jar 1. The infrared lamps 6 are arranged not only at the positions shown in Figure 6 but also all the way around the outside of the bell jar 1 at identical spacings. The infrared lamps 6 are backed by reflecting mirrors 4 so that all the infrared rays emitted from the infrared lamps 6 may reach the inside of the bell jar 1. The infrared lamps 6 and the reflecting mirrors 4 are supported on a support plate 8. The infrared lamps 6 are connected to a power supply 12. A temperature sensor is interposed in the bell jar 1 between the ingot 5 and the infrared lamps 6. A control unit 13, having a microprocessor, controls the power supply 12 in accordance with information from the temperature sensor. This control of the power supply 12, permits the ingot 5 to be heated and cooled quickly to the desired temperatures. The power supply 12 includes a thyristor. All the radiation of the infrared rays can be controlled either by wholly or partially turning off the power supply 12 or by limiting the current fed by the power supply 12.

The use of heat treatment by radiation, permits the ingot to be heated without physical contact. As a result, none of the aforementioned contaminations, mechanical stresses and temperature imbalances, which might otherwise by caused by contact with the apparatus arise. This method can control the temperature of the ingot more easily than other methods, such as the resistance heating method. This is partly because the heat transfer is effected by radiation and partly because the calorific output (of the infrared rays) can be controlled accurately and promptly.

The case in which the ingot of the silicon single crystal is to be annealed will now be described.

The ingot 5, which is supported in the contactless state in the quartz bell jar 1, as shown in Figure 6, is rotated. In this state, the ingot 5 is heated to a temperature between 1,200 and 1,350°C, for example, and held for 1 to 16 hours in the infrared rays coming from the infrared lamps 6. A higher temperature is desirable in order to enhance the annealing

effect. If the melting point of the semiconductor material is designated as T, the preferred annealing temperature is 0.85T to 0.95T. In the case of silicon, the annealing temperature should be higher than 1,200°C and ideally at 1,300°C ± 50°C. Figure 7 illustrates examples where an ingot is annealed at 1,200°C and another is annealed at 1,350°C. The ingot is heated at 1,200°C for 1 to 8 hours at 1,350°C for 0.5 to 3 hours.

Most of the causes for the formation of microdefect cores in the ingot are eliminated by that annealing treatment. Precipitates of 10 to 50 Å, which are formed during the growth of the ingot, are elliminated. Centres of stress concentration in the ingot due to the differences in temperature distribution are also eliminated. As a result, the distributions of the impurities such as carbon or heavy metals, the microdefect cores left in the ingot even after the annealing treatment, and oxygen, are made uniform in the ingot.

If the ingot is annealed at 1,300°c for about 16 hours, the oxygen concentration in the ingot can be reduced from 10^{18} atoms/cm^3 to 8×10^{17} atoms/cm^3 by diffusing oxygen to the outside of the ingot.

After the annealing treatments at those temperatures for the predetermined periods, the output of the infrared ray lamps 6 is reduced to cool the ingot quickly. The temperature programmes for this quick cooling treatment are illustrated in Figure 7.

The ingot is first cooled from the annealing temperature to about 1,100°C at rate of 10 to 15°C/min. Next, the ingot is cooled from about 1,100°C to about 300°C at a rate of 25 to 100°C/min. The rate the temperature drops per minute can be accurately controlled by controlling the total radiation of the infrared rays, as has been described above. The temperatures are the values which are sensed by the temperature sensor 14, i.e. the temperatures in the bell jar 1. The real temperatures of the ingot 5 are slightly higher than those values because of the large heat capacity of the ingot 5. The temperature of the ingot 5 changes with the temperature in the bell jar 1.

Few microdefect cores are generated at temperatures exceeding 1,000°c. The ingot is cooled slowly in order to limit side effects such as cracks due to cooling.

The generation of microdefect cores is promoted by temperatures below 1,100°C. In order to suppress that generation, the ingot is cooled quickly. If the ingot is cooled quickly from 1,100°C to 650°C, microdefect cores can be restrained from re-generating. Oxygen donors are generated within the temperature range of 650 to 380°C. In order to suppress this generation, the ingot is quickly cooled within that temperature range also. This makes is possible to prepare an ingot which has few microdefect cores and oxygen donors.

The temporary holding step at 300°C is to prevent the ingot 5 from cracking from the thermal stress during the quick cooling step. This may be done at any temperature lower than about 380°C. In the present embodiment, the ingot is held at 300°C so as to insure the suppression of the re-generation of the oxygen donors.

At temperatures below 300°C, the ingot can be further cooled after a predetermined time. The cooling rate in this case may be different from those of the aforementioned two-step quick cooling.

According to the embodiment discussed above, the ingot 5 of the silicon single crystal can be annealed at high temperatures in a contactless state. This makes it possible to melt the microdefect cores (i.e. the cores of oxygen precipitates) which are generated during the growth of the single crystal and the heat history in the furnace, without any fear of contamination. Due to the radiant heating system using infrared lamps 6, it is possible to cool the crystal more quickly than if a resistance heating system is used. As a result, it is possible to suppress the gathering of excess oxygen during the cooling step which causes microdefect cores to be generated.

The wafers, which are sliced off the single crystal ingot 5 and mirror-polished, contain very few oxygen precipitates even after the LSI process. This reduces significantly the generation of small dislocation loops and oxydation stacking faults.

An ordinary crystal usually has a microdefect density of 10^7 to 10^8 atoms/cm^3, whilst wafers fabricated by the process of the present embodiment may have a microdefect density of less than 10^5 atoms/cm^3. In this period when the temperature of the LSI process is dropping to a lower level and the crystal is used under severer conditions, the embodiment discussed above is particularly advantageous.

After the annealing step shown in Figure 7, the ingot may be annealed again at 600°C. This additional annealing step is performed to suppress a variation of resistances in various parts of the ingot. This is because, although most oxygen donors may be eliminated by use of the process of the present invention, a few oxygen donors may still be generated after the heat treatment at a temperature of 400°C to 600°C.

An ingot annealed by a process according to the present invention has remarkably few microdefect cores, (i.e., the cores of the oxygen precipitates) so a semiconductor element having excellent characteristics may be fabricated with a high yield.

Cracking may be prevented in the ingot by quicking cooling the ingot to a predetermined temperature after annealing and by holding it at a predetermined temperature for a predetermined time.

Although the present invention has been described in connection with specific embodiments, it is not limited to these embodiments but can naturally be modified in various ways.

For example, the cooling rate of the ingot can be changed. In particular the rate of 10°C to 15°C illustrated in Figure 7 may be changed. This rate may be changed to 25 to 100°c unless there is a possibility of the ingot cracking. Alternatively, the ingot may be cooled at a slow rate of 5 to 10 °C.

The annealing treatment illustrated in Figure 7 may be applied, not only to an ingot, but also to sliced wafers. In this modification, the wafers cannot be held in a state where they do not touch the apparatus so that this modification is less advantageous for suppressing the generation of mic-

rodefects and prevention of contamination than is the case in which the ingot itself is annealed.

Moreover, hydrogen and oxygen may be used as the atmospheric gas for the annealing treatment.

As an alternative to the use of infrared lamps, highfrequency coils or electromagnetic waves other than infrared rays can be used as the radiant heat source.

The end portion of the ingot 5 at the side of the seed 5a can be clamped and held by a quartz jig. This modified process is used when the seed 5a is broken and separated from the ingot 5. Nonetheless, this process is less advantageous in a wafer annealing treatment than in the case in which the ingot 5 is annealed by holding the seed 5a.

The description above is concerned with the case in which the present invention is applied to the annealing of a silicon single crystal ingot. However, the present invention should not be limited to this but can be applied to either a semiconductor of III-V groups such as gallium - arsenic (Ga - As) or gallium - phosphorous (Ga - P) or a semiconductor of II-V groups. The annealing temperature in this case is preferably 0.85Tk to 0.95Tk (where Tk is the melting point of the semiconductor).

CLAIMS

1. A process for fabricating a semiconductor material comprising:
(a) placing the semiconductor material in a container, by clamping the material in a holder;
(b) heating the semiconductor material by radient heat from a radient heat source; and
(c) cooling the semiconductor material.

2. A process according to claim 1, wherein the container is a bell jar, the holder is a chuck fixed to the bell jar, and the heat source is dispensed around the circumference of the bell jar.

3. A process according to claim 1 or claim 2, wherein the semiconductor material is cooled by controlling the radient heat source during step (c).

4. A process according to any one of the preceding claims, wherein the radient heat source includes a plurality of infrared lamps.

5. A process according to claim 4, wherein the semiconductor material is cooled during step (c) by controlling the electric currents flowing through the lamps.

6. A process according to any one of the preceding claims, wherein the container is filled with a non-oxidising atmosphere.

7. A process according to any one of the preceding claims, wherein the semiconductor material is clamped in the holder at a seed side of the material.

8. A process according to claim 7, wherein the semiconductor material is joined to a seed crystal and the seed crystal is claimed in the holder.

9. A process for fabricating a semiconductor material, comprising:
(a) heating and holding the semiconductor material at a high temperature;
(b) cooling the heated semiconductor material to a temperature of approximately 1,100°C;
(c) further cooling the cooled semiconductor material from the temperature of approximately 1,100°C to a temperature equal to or lower than 380°C at a rate of 25 to 100°C/min. ; and
(d) holding the further cooled semiconductor material at a temperature equal to or lower than 380°C.

10. A process according to Claim 9, wherein the cooling of step (b) is at a rate of 10 to 15°C/min.

11. A process according to claim 9 or claim 10, wherein the high temperature is at least 1200°C.

12. A process according to any one of the preceding claims wherein the semiconductor material is silicon.

13. A process according to any one of the preceding claims, wherein the semiconductor material is a single crystal ingot.

14. A process according to Claim 13, wherein the ingot has a diameter of at least 125 mm.

15. A process of fabricating a semiconductor material substantially as any one herein described with reference to Figures 5 to 7 of the accompanying drawings.

16. An apparatus for fabricating a semiconductor material comprising:
a container for receiving the semiconductor material;
a holder for suspending the semiconductor material in the container; and
a radient heat source for heating the semiconductor material.

17. An apparatus according to claim 16, wherein the container is a bell jar in the form of a hollow upright cylinder with a cover at the top of the cylinder hermetically sealing the bell jar.

18. An apparatus according to claim 17, wherein the holder is a chuck mounted on the cover of the bell jar.

19. An apparatus according to any one of claims 15 to 17, wherein radient heat source includes a plurality of infrared lamps, and wherein the container is made of transparent quartz.

20. An apparatus according to Claim 19, wherein the infrared lamps are arranged around the outer circumference of the container at a predetermined spacing from each other.

21. An apparatus according to claim 19 or claim 20 wherein the infrared lamps are backed with reflecting mirrors so that most of the infrared rays emitted from the infrared lamps are directed to said bell jar.

22. An apparatus according to any one of Claims 16 to 21, wherein the container has an inner contour similar to that of an ingot of the semiconductor material.

23. An apparatus according to any one of claims 16 to 22 wherein the holder is rotatable.

24. An apparatus according to any one of claims 16 to 23, being an upright type heat treating furnace for annealing the semiconductor material.

25. An apparatus for fabricating a semiconductor material substantially as herein described with reference to and as illustrated in Figure 6 of the accompanying drawings.

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